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## Introduction

The HSP50415 Wideband Programmable Modulator (WPM) is a quadrature amplitude modulator/upconverter designed for wideband digital modulation. The WPM combines shaping, halfband, and interpolation filters, a complex modulator, timing and carrier NCOs and dual DACs into a single package.

This application note describes the device configuration examples for processing a single UMTS standard channel per device. The example configuration information is formatted for use with the HSP50415Eval1 evaluation board and Microsoft® Windows® software.

Two UMTS device configurations have been provided in order to demonstrate both the single bit processing mode where 1-bit is computed per clock cycle, and the special two bit mode, where 2-bits are computed per cycle in the shaping filter. The special 2-bit mode allows increased input bit-width over the single bit mode.

## For All Examples

### Input Data Rate and Shaping Filter Requirements

The basic interpolation rates allowed through the shaping Filter are x4, x8 or x16. An optional decimate by 2 mode is available that subsamples the output of the filter thus reducing the interpolation rate by a factor of 2. Each filter multiplication is implemented as a series of shifts and adds thus constraining the maximum input symbol rate as follows:

symbolRateMax is the smaller of:

(CLK * 2 * 2^twoBitMode) / (#bits * interpolationRate)

and CLK/4

where CLK is the final sample rate clock (currently 100MHz max), #bits is the data bit width of a single channel and twoBitMode is the special processing mode where 2-bits are processed concurrently.

For UMTS, the symbolRateMax is computed as:

(100MHz*2*2^0) / (#bits * interpolationRate) or

selecting an interpolationRate of x4 we see the #bits must be less than 14 in order to accommodate the input symbol rate of 3.84MHz. The single bit mode configuration was selected to operate at a CLK rate of 92.16 MHz to provide for an overall interpolation rate of x24 for an input bit-width of 12-bits.

The special 2-bit mode configuration was also selected to operate at a CLK rate of 92.16 MHz to provide for an overall interpolation rate of x24, with the input bit-width increased to 16-bits.

### Shaping Filter Coefficients

The number of available FIR coefficients for UMTS at a 92.16MHz CLK rate is 96 for the single bit mode and 48 for the 2-bit mode per each individual I and Q filter. The filter coefficients were developed in Matlab® and the HSP50415 software was utilized to convert the coefficients from floating point to the bit-sliced-sum-of-products format utilized by the four 64x72bit shaping filter RAMs within the device.

### Data Flow

Data flows through the device as shown in figure 1. Data enters the shaping FIR at the symbol rate of 3.84MHz and exits at $f_S$* IP or 15.36MHz. The halfband filter interpolates by 2 to the $f_S$*IP*2 rate, or can be bypassed. Data enters the High Order Interpolation (HOI) filter and can be integer or non-integer interpolated, but always exits at the CLK rate. The digital logic runs at the CLK/2 rate and the HOI samples are computed two samples at a time in order to output at full rate. Please see the data sheet for the decimate by 2 shaping filter mode and additional device details.

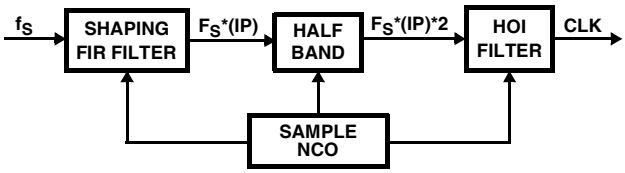


**FIGURE 1. CHANNEL RATES**

The shaping filter, halfband, and HOI filter combine to produce an overall interpolation through the device of CLK/$f_S$.

### File Formats

The evaluation board windows application program requires several types of input files to configure and load data into the board. Scripts are used to configure the evaluation board and for programming sequential actions. Java scripts (*.js) and Visual Basic scripts (*.vbs), created with any text editor, are supported. Specific file formats are required for each type of file, with examples provided in the evaluation software.

### Configuration Files *.js or *.vbs

Configuration files contain the evaluation board form contents in register command format. The header contains the set-up information required for the loader, followed by the reset commands and the software form registers output commands. Device commands are Puc.Poke, Puc.peek, setbits, clearbits, resetbits and modifybits. Evaluation board hardware commands which do not directly affect the device are Puc.Write and Puc.read. All ADDRESS, DATA, and MASK values are expressed in HEXADECIMAL. Additional insight on the command line window can be obtained by

using the forms to change bit fields and observing the corresponding commands being echoed in the command line window. Please see the evaluation board users manual for detailed information.

### *Coefficient Files *.coe or *.imp*

The coefficient files contain seven comment lines at the beginning, which are ignored by the loader, with each line thereafter containing one floating point coefficient per line. The magnitude of each coefficient must be less than one.

### *Pattern Files *.pat or *.imp*

The pattern file contains seven comment lines at the beginning, which are ignored by the loader, with each line thereafter containing two floating point numbers with values that must be less than 1. The first number is for the I data, and the second is for the Q data.

### *Clock Rates*

The CLK rates specified for the examples may vary from the oscillator installed in the evaluation board position U6. The evaluation boards are supplied with an 100MHz oscillator. Please ensure that you remove the U6 oscillator and utilize the J4 clock input SMA connector in order to support the specific examples shown herein. Please see the reference documents section of the FN4859 manual to obtain an evaluation board schematic and other applicable documents.

## *Example Configurations*

### *UMTS-single bit mode*

The device is configured for outputting one channel of UMTS. The 12-bit I and 12-bit Q data is input via the parallel DIN<15:0> input utilizing the 2xSYMCLK output tied back to the DATACLK input. The input symbol rate is 3.84MHz. The shaping FIR is programmed to single bit mode with interpolate by x4 and a symbol span of 24, providing 96 filter taps. The filter frequency response is shown in Figure 2. The halfband filters and sinX/X compensation filters are enabled. The output carrier frequency is set to 10.7MHz. The DAC parameters are set to scale to 1.0, round to 12-bits at output and no offset. The analog and digital PLLs are disabled. The analog performance of the device is shown in Figure 3, utilizing the internal device DAC's. The stimulus file is 511 samples of pseudo random QPSK data. It is important to note that the CLK rate does not have to be a integer multiple of the Sample Frequency, and that non-integer interpolation through the high order interpolation filter allows any CLK rate to be accommodated.

**TABLE 1. UMTS CONFIGURATION**

| | |
|---|---|
| Clock Rate CLK = | 92.16MHz |
| Sample Frequency $f_S$ = | 3.84MHz |
| Configuration File: | UMTS_1_bit.js |
| Filter File: | UMTS_BLK_4x.imp |
| Stimulus File: | qpskpn.imp |

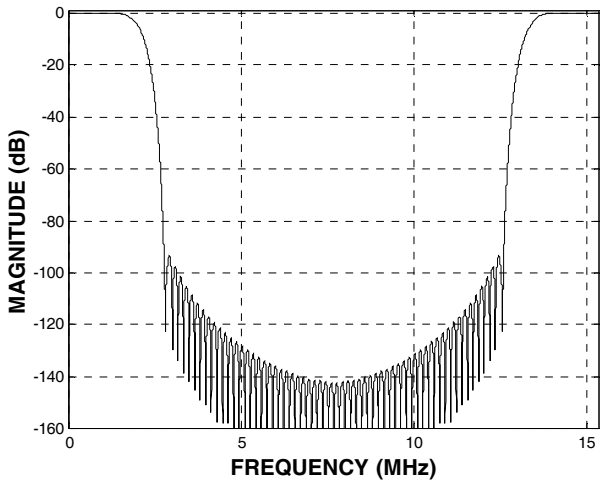


**FIGURE 2. SHAPING FILTER FREQ. RESPONSE**

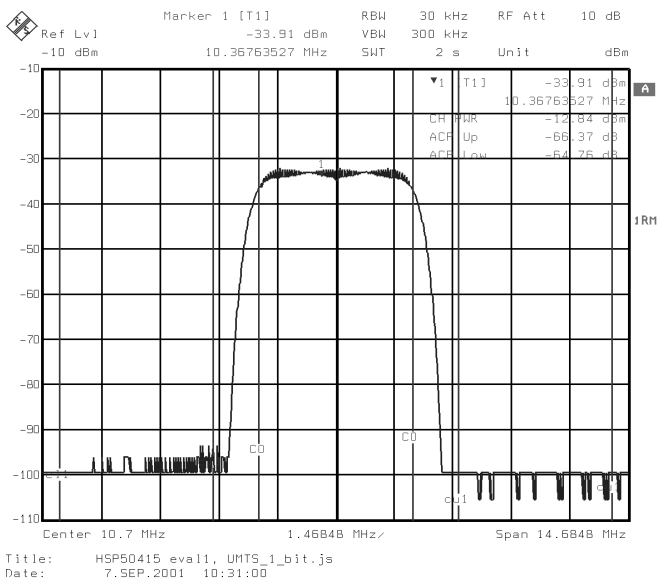


**FIGURE 3. ANALOG SPECTRUM**

In order to work within the spectrum analyzer equipment limitations, the CLK frequency was reset to 92.16MHz/2, which resulted a reduction in the sample rate to 1.92MHz, and a reduction of the center frequency to 5.35MHz. The adjacent channel power standard is set to W-CDMA 3GPP FWD with the measure filter set to RRC, the reference filter set to RC, and the Alpha/BT set to 0.22. The vector analyzer output is shown in Figure 4.

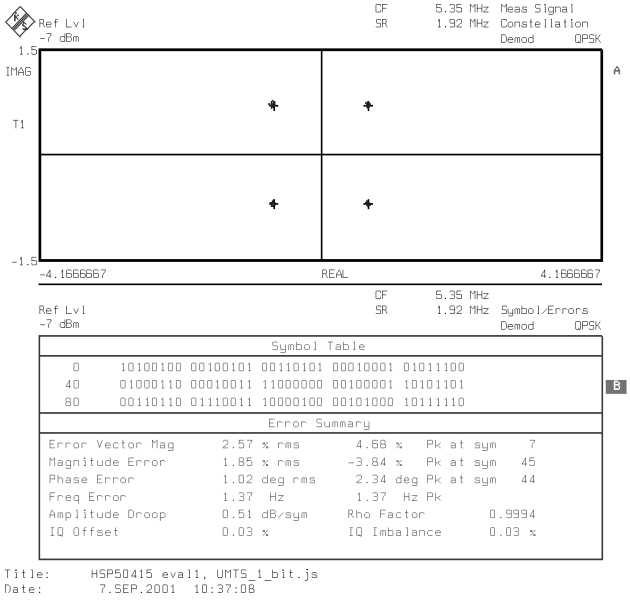


**FIGURE 4. VECTOR ANALYSIS**

### *UMTS-Two bit mode*

The device is configured for outputting one channel of UMTS. The 16-bit I and 16-bit Q data is input via the parallel DIN<15:0> input utilizing the 2xSYMCLK output tied back to the DATACLK input. The input symbol rate is 3.84MHz. The shaping FIR is programmed to two bit mode with interpolate by x4 and a symbol span of 12, providing 48 filter taps. The filter frequency response is shown in Figure 5. The halfband filters and sinX/X compensation filters are enabled. The output carrier frequency is set to 10.7MHz. The DAC parameters are set to scale to 1.0, round to 12-bits at output and no offset. The analog and digital PLLs are disabled. The analog performance of the device is shown in Figure 6, utilizing the internal device DAC's. The stimulus file is 511 samples of pseudo random QPSK data.

**TABLE 2. UMTS CONFIGURATION**

| | |
|---|---|
| Clock Rate CLK = | 92.16MHz |
| Sample Frequency $f_S$ = | 3.84MHz |
| Configuration File: | UMTS_2_bit.js |
| Filter File: | UMTS_48t0.imp |
| Stimulus File: | qpskpn.imp |

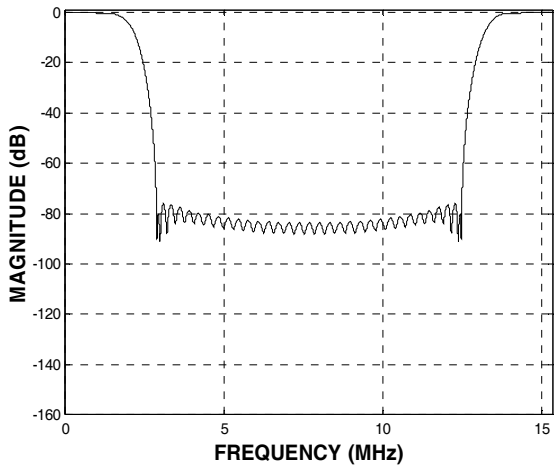


**FIGURE 5. SHAPING FILTER FREQ. RESPONSE**

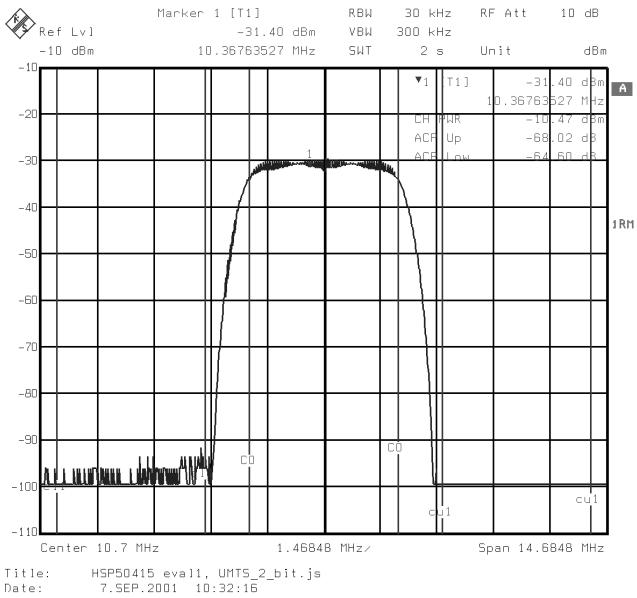


**FIGURE 6. ANALOG SPECTRUM**

In order to work within the spectrum analyzer equipment limitations, the CLK frequency was reset to 92.16MHz/2, which resulted a reduction in the sample rate to 1.92MHz, and a reduction of the center frequency to 5.35MHz. The adjacent channel power standard is set to W-CDMA 3GPP FWD with the measure filter set to RRC, the reference filter set to RC, and the Alpha/BT set to 0.22. The vector analyzer output is shown in Figure 7.

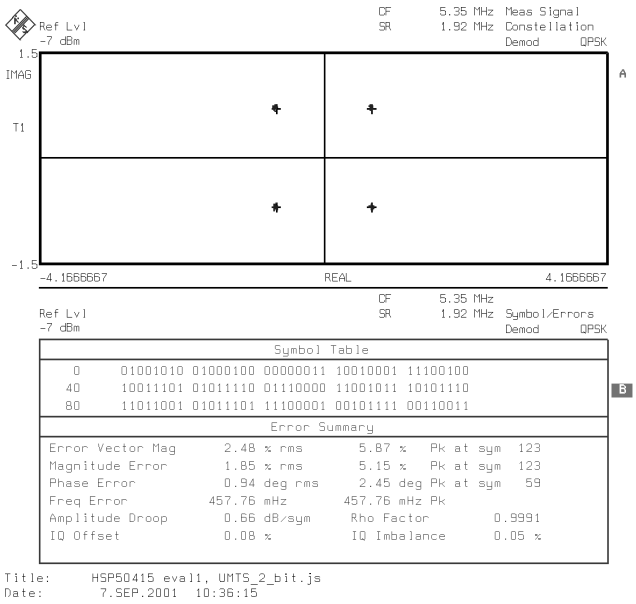


**FIGURE 7. VECTOR ANALYSIS**